SYLLABUS

1. Data about the program of study

1.1 Institution	Technical University of Cluj-Napoca
1.2 Faculty	Faculty of Electronics, Telecommunications and information Technology
1.3 Department	Bases of Electronics
1.4 Field of study	Electronic Engineering, Telecommunications and Information Technologies
1.5 Cycle of study	Bachelor of Science
1.6 Program of study / Qualification	Applied Electronics / Engineer
1.7 Form of education	Full time
1.8 Subject code	49.10

2. Data about the subject

2.1 Subject name							
2.2 Subject area	Theoretical area Methodological area Analytic area						
2.3 Course responsible	Assoc. Prof. Albert Fazakas – Albert.Fazakas@bel.utcluj.ro						
2.4 Teacher in charge with seminar / laboratory / project	Assoc. Prof. Albert Fazakas – Albert.Fazakas@bel.utcluj.ro						
2.5 Year of study	IV	2.6 Semester	I	2.7 Assessment	E	2.8 Subject category	DS/DOP

3. Estimated total time

3.1 Number of hours per week	4	of which: 3.2 course	2	3.3 seminar / laboratory	2
3.4 To Total hours in the curriculum	56	of which: 3.5 course	28	3.6 seminar / laboratory	28

Distribution of time	hours
Manual, lecture material and notes, bibliography	8
Supplementary study in the library, online specialized platforms and in the field	8
Preparation for seminars / laboratories, homework, reports, portfolios and essays	46
Tutoring	4
Exams and tests	3
Other activities:	0

3.7 Total hours of individual study	69
3.8 Total hours per semester	125
3.9 Number of credit points	5

4. Pre-requisites (where appropriate)

4.1 curriculum	Digital Integrated Circuits, Digital Systems
4.2 competence	Analysis and Design of Digital Systems CAD tools for analysis and design of Digital Systems

5. Requirements (where appropriate)

5.1. for the course	Cluj-Napoca, classroom equipped with video projector
5.2. for the seminars / laboratories / projects	Cluj-Napoca, classroom equipped with computer network, Vivado Design System software, 7-Series and Zynq-based FPGA development systems, specific peripheral modules

6. Specific competences

Professional competences	C3. Application of knowledge, concepts and basic methods related to Computing Systems Architectures, microprocessors, microcontrollers, programming techniques and languages • C3.3 Solving practical problems that include algorithms and data structure elements and use microprocessors or microcontrollers • C3.4 Software elaboration, starting from specifications up to execution, debug and testing, written in a general or processor-specific programming language, • C3.5 Elaboration of projects involving hardware-software co-existence C4. Design and use of simple hardware and software applications, specific to the Applied Electronics domain • C4.1 Definition of concepts, principles and methods used in computer Programing, High-Level Description Languages, CAD design tools, microcontrollers, Programmable and Reconfigurable Electronic Circuits • C4.2 Interpreting and explaining the specific requirements for hardware and software structures in the domains related to high-level languages and reconfigurable hardware architectures • C4.4 Use of adequate performance criteria for evaluating dedicated systems which use medium or reduced complexity computing architectures, by simulation or hardware testing • C4.5 Design of dedicated electronic systems containing microcontrollers, FPGA or other computing systems in the Applied Electronics domain
Cross competences	CT1. Methodic analysis of the problems encountered during the activity, identifying those elements for which well-known solutions exists, ensuring in this way successful completion of the professional tasks. CT3. Upgrade to the new technologies, professional and personal development by continuous forming, using electronic and printed documentation and specialized software

7. Discipline objectives (as results from the key competences gained)

7.1 General objective	Professional skill development in the field of FPGA/SoC-based Digital Systems Design, using HDL description languages and reconfigurable microprocessor systems
7.2 Specific objectives	Theoretical knowledge of FPGA/SoC structures, understanding their possibilities and limitations Knowledge of specific CAD software tools for FPGA - and SoC – based systems Knowledge of Hardware Description Languages and their efficient usage for Digital Design creation Developing skills for testing, debug and optimization of digital projects for speed and/or area

	Gaining knowledge of how to use the FPGA-specific digital components efficiently: BRAM, DDR controllers, Clocking Circuits etc. Developing systematic design and methodologies that combine analysis simulation and practical experiments

8. Contents

8.1 Lecture (syllabus)	Teaching methods	Notes
1. Introduction. What is FPGA? State-of-the Art in FPGA – and SoC- based systems and development tools.	Presentation, heuristic conversation, exemplification, problem presentation and solving, case studies	Onsite: Video projector and blackboard are used Online: Specific collaboration platform, presentations using shared screen
2. Programmable Logic Device structures: PLA, PAL, GAL, CPLD. The FPGA structure principle. Basic elements in FPGA.		
3. FPGA systems design methodology. Steps during design procedure. Design verification methods.		
4. FPGA-specific digital design techniques (1). Propagation delay time definitions. Propagation delay time calculus		
5. FPGA-specific digital design techniques (2). Logic hazard. Synchronous design techniques. Synchronizing external signals. Applying FIFO.		
6. Digital synthesis. Design optimization techniques used by the synthesizer. FSM types and description techniques		
7. Microprocessor systems based on Microblaze and ARM A9 processor. The AMBA – based architecture: AXI.		
8. The AXI lite protocol. Processor to peripheral communication model. Accessing peripheral devices using internal registers and device drivers.		
9. The Microblaze and ARM A9 interrupt systems I. Interrupt controllers. Configuring interrupts in software.		
10. The Microblaze and ARM A9 interrupt systems II. Real-time process control.		
11. Processor peripherals HDL structure. Creating and connecting Custom Peripherals. Port and parameter propagation through the peripheral hierarchy.		
12. FPGA clocking and clock distribution, Regional and global clocks. Components used for clock generation and management. Clock related timing constraints.		
13. Practical aspects of FPGA boards: FPGA configuration. The JTAG controller. FPGA power lines and power sequencing. Hardware monitoring: The XADC component.		
14. Synthesis of digital circuits using High-Level Synthesis – HLS language		

Bibliography
1. Albert Fazakas, FPGA Systems, PowerPoint presentations, 2023
2. Steve Kilts, "Advanced FPGA Design", John Wiley and Sons, 2007
3. Xilinx inc., „Artix-7 FPGAs Data Sheet: Overview", DS180 (v2.6) February 27, 2018, www.xilinx.com
   - Datasheets and User Guides for the 7-Series FPGA: **DS181, UG470..UG476**
4. Xilinx inc., „Zynq-7000 SoC Data Sheet: Overview", DS190 (v1.11.1) July 2, 2018, www.xilinx.com
   - Datasheets and User Guides for the 7-Series ZynQ SoC, : UG585, DS191, DS187, UG1165, UG873

8.2 Laboratory	Teaching methods	Notes
1. Introduction Familiarizing with the Xilinx Vivado Design Environment and the Digilent Nexys4DDR and Zybo development boards.	Practical experiment and proof of concepts, teamwork	Onsite: FPGA- and SoC- based boards, laboratory equipment, Vivado software, video projector and blackboard are used. Online: Specific collaboration platform, Vivado software simulator, virtual access to development boards
2. Simulating HDL projects. Creating testbenches. Simulation messages. Extended testbench instructions		
3. Hierarchizing HDL projects. Creating hierarchical projects in Vivado. IP core.		
4. FSM descriptions in HDL. FSM applications example.		
5. FSM applications for standard serial peripheral communication (SPI, UART, I2C)		
6. Processor base system on Microblaze and ARM A9. The AXI lite protocol. Simulating microprocessor systems.		
7. Accessing processor peripherals by internal registry access and by device drivers.		
8. Microblaze and ARM A9 interrupt hardware and software configuration.		
9. Process control using Timer and interrupts. Real-time response.		
10. Creating custom peripheral devices I. Checking the HDL code. Access to peripheral device registers.		
11. Creating custom peripheral devices II. Applications with the custom peripheral device.		
12. Hardware project debugging from inside the FPGA chip. Preparing for hardware debugging. The Integrated Logic Analyzer (ILA) and Virtual I/O (VIO cores		
13. FPGA configuration examples. Creating and deploying FPGA configuration files to external memory.		
14. Clocking in FPGA. The MMCM2E_ADV and PLL2E_ADV IP cores. Example: VGA interface for various resolutions. Propagation time dalay constraints.		

Bibliography
1. Albert Fazakas, FPGA Systems, laboratory tutorials, 2023
2. Digilent inc., „Nexys4DDR User Manual", rev. C, April 11, 2016,

https://reference.digilentinc.com/_media/nexys4-ddr:nexys4ddr_rm.pdf
3. Digilent inc., „Nexys4DDR Schematics", rev. C, 2014, https://reference.digilentinc.com/_media/nexys4-ddr:nexys_4_ddr_sch.pdf
4. Digilent inc., „Zybo Z7 Board Reference Manual", Revised February 21, 2018, https://reference.digilentinc.com/_media/reference/programmable-logic/zybo-z7/zybo-z7_rm.pdf
5. Digilent inc., „Zybo Z7 Board Schematic", Rev. B.2, Copyright 2017, https://reference.digilentinc.com/_media/reference/programmable-logic/zybo-z7/zybo_z7_sch-public.pdf
6. Xilinx inc., „Vivado Design Suite User Guide: Getting Started", UG910, https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_4/ug910-vivado-getting-started.pdf
7. Xilinx inc., „Vivado Design Suite User Guide: Using the Vivado IDE", UG893, https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_4/ug893-vivado-ide.pdf

9. Bridging course contents with the expectations of the representatives of the community, professional associations and employers in the field

The discipline content and the acquired skills are in agreement with the expectations of the professional organizations and the employers in the field, where the students carry out the internship stages and/or occupy a job (in the field of digital and embedded system design,simulation and testing), and the expectations of the national organization for quality assurance (ARACIS).

10. Evaluation

Activity type	10.1 Assessment criteria	10.2 Assessment methods	10.3 Weight in the final grade
10.4 Course	The level of acquired theoretical knowledge and competences	C – Formative in-presentation evaluation (answer to the questions asked by the teacher) OE – Oral exam for overall evaluation (solving theoretical problems)	C (max. 1 p) OE (max. 10 pts.), 40%
10.5 Seminar/ Laboratory	The level of acquired practical abilities	LR – 4 Laboratory Reports (solving Laboratory Exercises) PR – Project Reports (elaborating parts of the project) MP – Practical miniproject implemented on FPGA or SoC development board, using specific CAD tools	LR1, LR2, LR3, LR4 (max. 10p) PR1, PR2, MP (max. 10 pts.), 60%
10.6 Minimum standard of performance			

Quality aspects:

Minimal knowledge level:

- ✓ Knowledge about the FPGA and SoC principle, specific CAD tools, hardware and software design creation
- ✓ Project verification and debugging

Quantity aspects:

- ✓ Passing all the Laboratory Works and obtaining passing grade on all the Laboratory Reports (LR)
- ✓ Passing the Project (PR1, PR2, MP) and Oral Exam (OE), minimal grade: 5
- ✓ Final grade formula: = 0.4OE + 0.6MP + C

Date of filling in:	Responsible	Title Surname NAME	Signature
30.06.2023	Course	Assoc. Prof. Albert FAZAKAS, PhD eng	
	Applications	Assoc. Prof. Albert FAZAKAS, PhD eng	

Date of approval in the Department of Bases of Electronics: 11.07.2023

Head of Department
Prof. Sorin HINTEA, PhD eng.

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Date of approval in the Council of Faculty of Electronics, Telecommunications and Information Technology: 12.07.2023

Dean
Prof. Ovidiu POP, PhD eng.

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